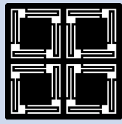

HYSITRON®

APPLICATION NOTE

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Thermal Expansion Study in a TSV-Structure

In-Situ Imaging From 23°C to 400°C in a Controlled Sample Micro-Environment

Introduction

The 3D integration of semiconductor chips requires engineering design that manages the stresses in the stacked structure. These stresses are unavoidable as materials with different coefficients of thermal expansion (CTE) are used in the construction of 3D integrated circuits. Thermal cycling during the device's function or an annealing step during production can induce stresses that potentially lead to failure of the device. A simple example of a system subjected to such stresses is a through silicon via (TSV). A TSV typically consists of a 5 to 25µm diameter hole in a Si wafer that ultimately connects between the front and back of the wafer. Cu is electrochemically deposited in the hole to allow electrical conduction (Fig. 1).

Si has a CTE of 2.6ppm/°C while Cu has a CTE of 16.7ppm/°C. This mismatch causes stresses at the interface between the materials that changes with changing temperature. The Si and Cu structures are exposed to temperature ranges up to 400°C during production and life of the device. It is therefore necessary to study the behavior of the Si and Cu at these temperatures.

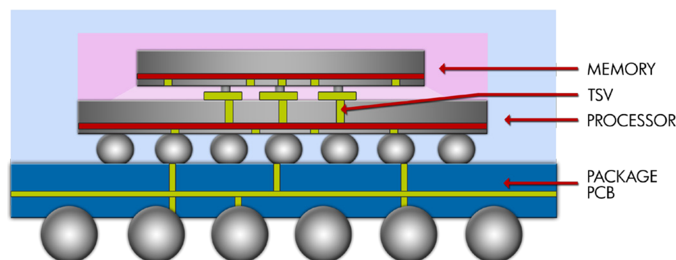


Figure 1: 3D-IC design showing a memory chip connected to a processor chip with TSVs.

In-Situ Imaging

The **TI 950 TriboIndenter®** offers *in-situ* SPM quantitative topographical imaging by raster-scanning an indenter probe over a sample surface using extremely low contact forces (typically 0.07 to 2µN). In combination with a temperature control stage, *in-situ* imaging allows measurement of the out-of-plane expansion of a Cu TSV at different temperatures and quantification of the reversible recovery when cooling back to room temperature.

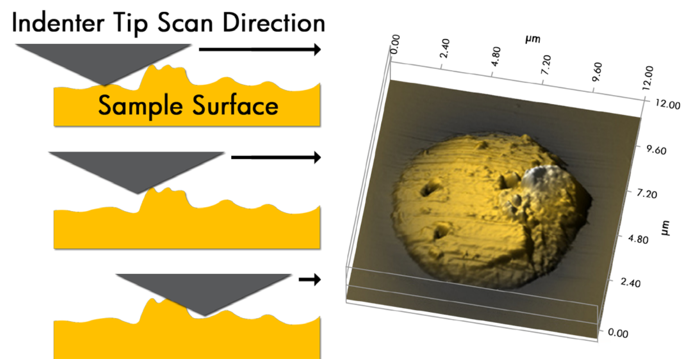


Figure 2: Schematic representation of the principle of *in-situ* SPM imaging. The 3D image on the right shows a TSV at 400°C surrounded by the Si wafer surface.

Heating and Cooling

The NOVA temperature control stage uses resistive heating elements to reach temperatures up to 400°C in less than 60. The temperature of the sample is controlled using a precisely calibrated PID feedback loop. A gas blend of Argon (95%) and Hydrogen (5%) was used to prevent oxidation of the Cu surface, which was observed beginning at roughly 200°C in ambient atmosphere.

Results

In-situ images of TSVs with 10µm diameter that had been exposed to a 420°C post-plating anneal were captured at different temperatures (23°C prior to heating, 200°C, 300°C, 400°C, 23°C after heating). The images revealed the reversible expansion of the TSV and the plastic deformation induced by the thermal stresses. Section profiles of TSVs in Fig. 3 show that the height of Cu increased dramatically between 300° and 400°C. Fig. 4 shows topographical images of TSVs under three conditions, and the stressed state of the structure is evidenced in the images by bowing of the Si surface around the TSV. Sections of the SPM images in Fig. 4 are analyzed in Fig. 5. The reversible thermal expansion of 55nm is found by comparing the profile at 400°C to the profile at 23°C after the heating experiment. Heating to 400°C induced sufficient thermal stresses that the yield strength of the Cu was exceeded, causing Cu to be "pumped" out of the TSV. This plastic flow increased the height of the TSV by 175nm.

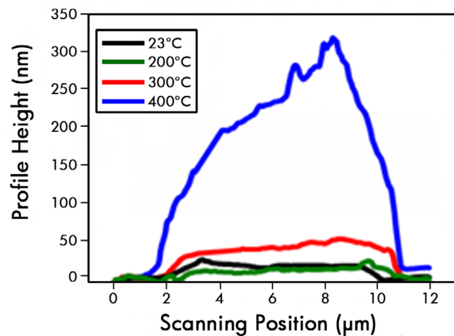


Figure 3: Profiles of the TSV at different temperatures. The extensive deformation being the superposition of the Cu extrusion and Si deformation has been observed between 300° and 400°C.

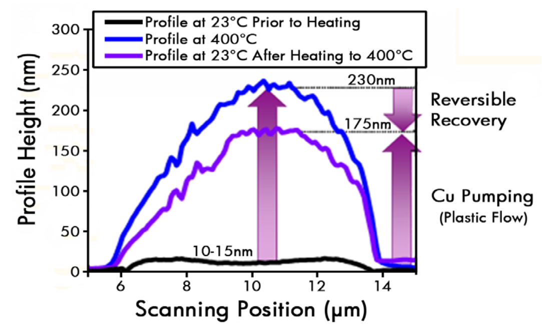


Figure 5: Comparison of height profiles through the TSV center (dotted lines in Fig. 4) as measured before, during, and after heating to 400°C.

23°C
Prior to Heating

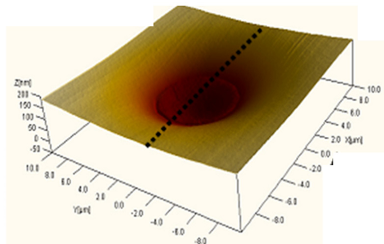
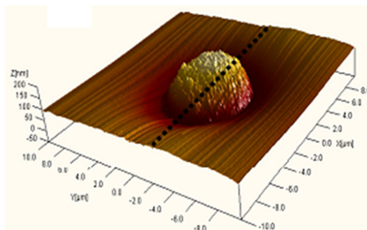


Image at 400°C



23°C
After Heating

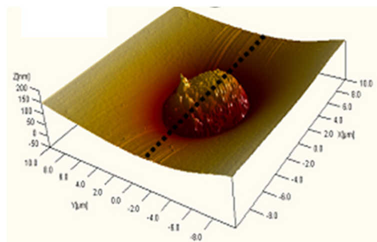


Figure 4: 3D topographical images of a TSV cycled from 23°C to 400°C and back to 23°C. The images show plastic deformation of the TSV at elevated temperature and reversible recovery upon cooling.

Conclusion

Stresses inside semiconductor devices are largely affected by the mismatch in CTE among the devices' various components. With large temperature changes, the stresses developed can be sufficient to cause plastic flow as well as deformation of the components, which alters the shape of the engineered structure. In the present example, thermally induced plastic flow caused a TSV to extend its height by 175nm while the reversible expansion was only 55nm. The performance of these structures can be altered through engineering by controlling the microstructure and design of the TSVs. Factors such as crystal orientation, grain size, and composition can change the strength and expansion rates of the materials in the system. *In-situ* SPM imaging at different temperatures allows quantification of TSV deformation during thermal cycling.

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